On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part II—Effect of Drain Voltage

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***Abstract*—In this paper, we study the effect of the drain voltage on the threshold voltage extraction in long-channel MOSFETs by the transconductance change and transconductance-to-current ratio change methods, using analytical modeling and experimental data obtained on advanced UTB SOI MOSFETs. It is shown that, although these two methods have the same physical background, they feature radically different behaviors with respect to the drain voltage effect. In particular, the transconductance change method yields a threshold voltage value, which regularly increases with drain voltage, and interpretation, as well as analytical expression for this dependence, is provided. In contrast, for the transconductance-to-current ratio change method, the increase of the extracted threshold voltage value with drain voltage is smaller and rapidly saturates; hence, the threshold voltage extraction is more stable and reliable. Modeling derivations are found to be in excellent agreement with measurements on long-channel UTB SOI MOSFETs as well as 2-D simulations.**

***Index Terms*—MOSFET threshold voltage extraction, transconductance change method, transconductance-to-current ratio, unified charge control model (UCCM).**

I. Introduction

THE ACCURATE determination of the MOSFET threshold voltage $V_{\rm TH}$ is essential for CMOS device/circuit design and modeling, particularly for advanced ultralow-power devices. Among numerous $V_{\rm TH}$ extraction techniques [1]–[5], the transconductance change method [3] is recognized as one of the most useful and accurate because it is considered to be unaffected by mobility degradation and series resistance effects. In this method, threshold voltage is defined from the position of the maximum of the transconductance (g_m) derivative in respect to the gate (V_g) voltage, i.e., the second derivative of the drain current $(d^2I_d/dV_g^2 \equiv dg_m/dV_g)$ measured in the linear operation regime, typically with an upper limit of the drain voltage of ~0.1 V. By this definition, the threshold voltage of an ideal device is a point where the second derivative of the inversion charge is at maximum. The aforementioned criterion is shown to be very suitable to represent threshold voltage behavior in advanced SOI devices [5].

Previously, we have proposed a method named the transconductance-to-current ratio change method [6], which relies on the same $V_{\rm TH}$ criterion, but in which the threshold voltage is determined from the position of the maximum of the $[-d(g_m/I_d)/dV_g]$ versus gate voltage function. The advantage of this method over the dg_m/dV_g method is its lesser sensitivity to second-order effects, such as V_g-dependent mobility and series resistance effects. In particular, in the companion paper [7], it is shown that, for the same mobility variation, the error in the $V_{\rm TH}$ extraction is much smaller (by 1.5–2 orders of magnitude) for the $d(g_m/I_d)/dV_g$ method than for the dg_m/dV_g method.

The purpose of this paper is to study the effect of the drain voltage value on the $V_{\rm TH}$ extraction by dg_m/dV_g and $d(g_m/I_d)/dV_g$ methods in long-channel MOSFETs. Preliminary results showing different behaviors of the dg_m/dV_g and $d(g_m/I_d)/dV_g$ methods with respect to the drain voltage effect have been reported in [8]. In this paper, we present a more detailed analysis of the conditions corresponding to the maxima of dg_m/dV_g and $[-d(g_m/I_d)/dV_g]$ versus gate voltage functions at various drain voltages, using the unified charge control model (UCCM) [9], and derive analytical expressions for the peak position shifts for dg_m/dV_g and $[-d(g_m/I_d)/dV_g]$ with drain voltage. Modeling predictions are compared with 2-D numerical simulation results and experimental data for long-channel ultrathin-body (UTB) SOI MOSFETs.

II. Experimental Results

The experimental data have been obtained on n-channel UTB with ultrathin buried oxide (UT2B) SOI MOSFETs fabricated at CEA-LETI. The devices featured an undoped channel with the silicon film thickness $t_{\rm Si} = 7$ nm and buried oxide thickness

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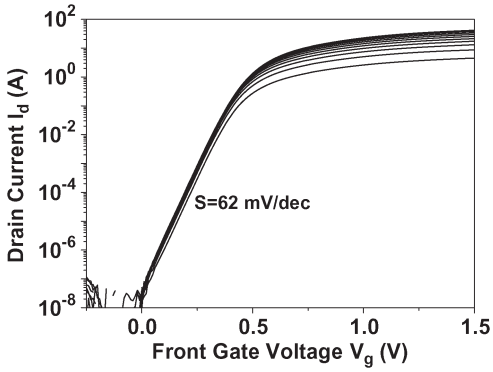

Fig. 1. Drain current versus gate voltage characteristics of a 10-μm-long UT2B SOI MOSFET measured for various drain voltages varying from 10 to 100 mV with a 10-mV step, showing the variation of the subthreshold (diffusion) current with drain voltage when $V_d < 2{-}3\ kT/q$ ($W = 10\ \mu$m, $V_{\rm sub} = 0$).

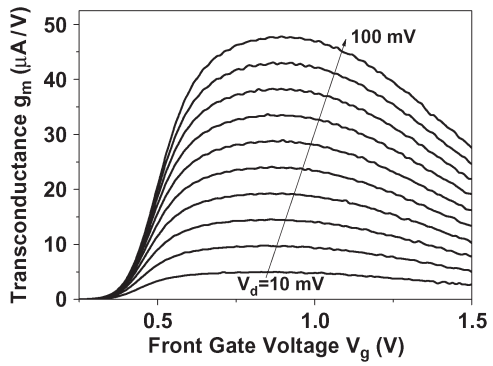

Fig. 2. Evolution of the experimental transconductance versus gate voltage curves with variation of the drain voltage from 10 to 100 mV for the device of Fig. 1. The drain voltage step is 10 mV ($L = 10\ \mu$m, $W = 10\ \mu$m, $V_{\rm sub} = 0$).

$t_{\rm BOX} = 10$ nm. Details of fabrication processes can be found in [10]. The gate stack consisted of a HfSiON gate dielectric with an equivalent oxide thickness of 1.3 nm, and a TiN gate electrode. Measurements have been performed at room temperature and zero substrate bias ($V_{\rm sub} = 0$). The V_g step in the measurements was 10 mV. In this paper, we concentrated on the long-channel devices.

Fig. 1 presents the $I_d(V_g)$ characteristics of the 10-μm-long device for various drain voltages V_d varying from 10 to 100 mV with a 10-mV step. Note the near-ideal subthreshold swing $S =$ 62 mV/dec and the variation of the subthreshold (diffusion) current with drain voltage when V_d is less than 50–70 mV. The corresponding $g_m(V_g)$ curves are shown in Fig. 2. One can see that the rising edge of the $g_m(V_g)$ curves tends to saturate with V_d, whereas in a strong inversion region, g_m linearly increases with V_d. As a result, the inflection point on $g_m(V_g)$ curves, which corresponds to the maximum dg_m/dV_g, gradually moves to higher V_g values.

Fig. 3 shows the g_m/I_d-versus-V_g curves for the same device for different V_d's varying from 10 to 100 mV in Fig. 3(a) and from 100 mV to 1.2 V in Fig. 3(b). It is seen that the g_m/I_d curves are only slightly affected by the drain voltage and tend to saturate with V_d. The variation of the falling edge of the g_m/I_d curves is pronounced only for $V_d < 100$mV [see

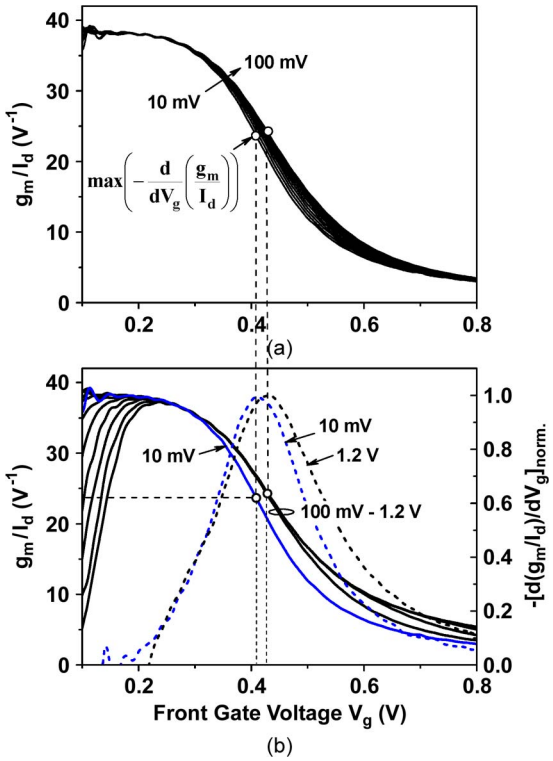

Fig. 3. g_m/I_d versus V_g curves for the 10-μm-long MOSFET for different V_d's. (a) From 10 to 100 mV with a 10-mV step. (b) 10 mV and V_d varying from 100 mV to 1.2 V with a 100-mV step. Dashed lines in Fig. 3(b) show normalized $-d(g_m/I_d)/dV_g$ characteristics at $V_d = 10$ mV and 1.2 V ($V_{\rm sub} = 0$).

Fig. 3(a)], whereas at higher V_d, the g_m/I_d curves in the range of inflection merge together [see Fig. 3(b)].

Fig. 4(a) shows the evolution of dg_m/dV_g and $-d(g_m/I_d)/dV_g$ characteristics with increasing V_d from 10 to 100 mV. As V_d increases, the position of the maximum of dg_m/dV_g regularly shifts to higher V_g values. The behavior of the peak position of $-d(g_m/I_d)/dV_g$ is completely different: Its shift is smaller and rapidly saturates with V_d. This is more clearly seen in Fig. 4(b) where, for ease of comparison, dg_m/dV_g and $d(g_m/I_d)/dV_g$ curves are normalized to their peak values and in Fig. 5 where the position of the maximum of both is plotted as a function of V_d. A higher $V_{\rm TH}$ value given by the dg_m/dV_g method compared to $d(g_m/I_d)/dV_g$ at very low drain voltage ($V_d = 10$ mV) in Figs. 4 and 5 is attributable to the impact of the mobility variation around the threshold due to Coulomb scattering at interface charges [7]. As is seen from Figs. 4 and 5, at $V_d < 70{-}80$ mV, the peak position of $-d(g_m/I_d)/dV_g$ slightly shifts with V_d, whereas at $V_d > 80{-}100$ mV, it becomes independent of V_d. The total shift of the peak position of $-d(g_m/I_d)/dV_g$ does not exceed 20 mV. In contrast, the gate voltage of the maximum of dg_m/dV_g increases monotonically with V_d and saturates only when the device enters the saturation regime.

Thus, from the experimental data, it is evident that the drain voltage has a completely different effect on the behavior of $g_m(V_g)$ and $g_m/I_d(V_g)$ characteristics and, thereby, on the peak positions of their derivatives. In the following sections, we analyze the origin of these different effects.

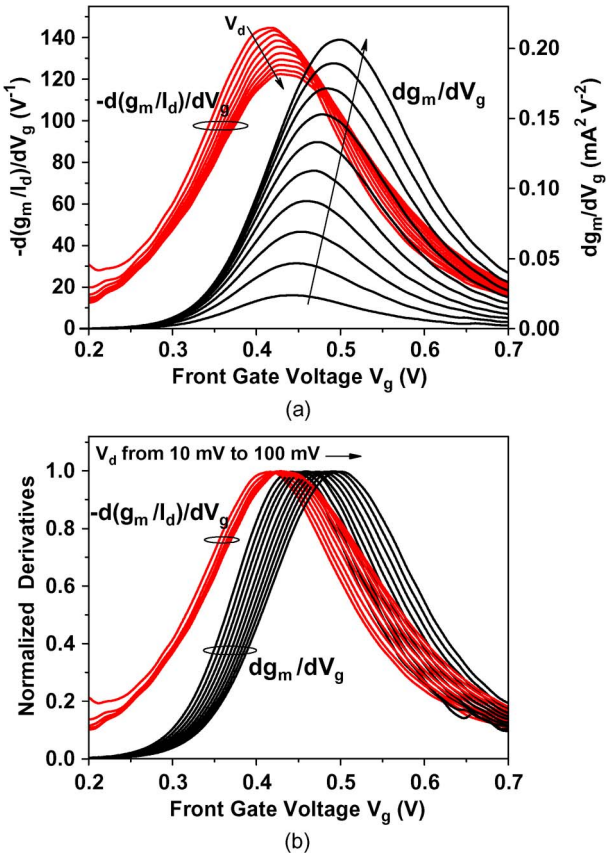

Fig. 4. (a) Experimental dg_m/dV_g and $-d(g_m/I_d)/dV_g$ versus gate voltage characteristics for the 10-μm-long n-channel MOSFET for different V_d's varying from 10 to 100 mV with a 10-mV step. (b) dg_m/dV_g and $d(g_m/I_d)/dV_g$ curves for different V_d's normalized to their peak values ($V_{\rm sub} = 0$).

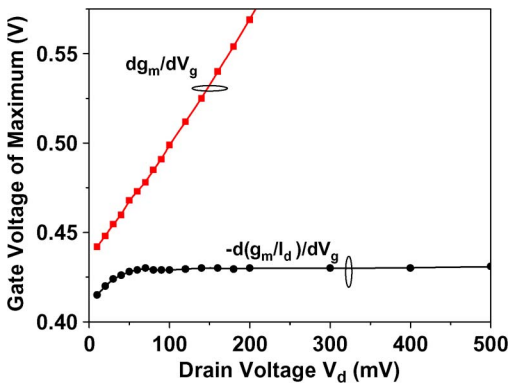

Fig. 5. Gate voltage corresponding to the maxima of experimental dg_m/dV_g and $-d(g_m/I_d)/dV_g$ characteristics plotted as a function of the drain voltage for the 10-μm-long MOSFET ($V_{\rm sub} = 0$).

III. Analysis of Drain Voltage Effect Using Analytical Modeling

For better understanding the origin of the aforementioned V_d effects, we performed an analysis of the behaviors of the $g_m(V_g)$ and $g_m/I_d(V_g)$ characteristics and their derivatives with drain voltage and derived analytical expressions for the V_d-induced shifts of the peak positions of dg_m/dV_g and $-d(g_m/I_d)/dV_g$.

We consider a long n-channel MOSFET with a constant mobility and ignore quantum and short-channel effects. The source potential is assumed to be zero ($V_s = 0$). Just as in the companion paper [7], we define the reference threshold voltage $V_{\rm TH}$ to be the gate voltage at which $d^2N_{\rm inv}/dV_g^2$ is maximum (where $N_{\rm inv}$ is the inversion carrier density per unit area for the uniform channel). Similar to the companion paper [7], in the analysis of the V_d effect, we use findings of the UCCM [9].

In the case of the position-dependent channel potential, according to the UCCM, for any point of the channel, one can write the relationship

$$V_g - V_{\rm TH} - nV_{\rm ch} = nV_T \ln \frac{N_{\rm ch}}{N_0} + a \cdot (N_{\rm ch} - N_0) \qquad (1)$$

where V_g is the applied gate voltage, $V_{\rm TH}$ is the threshold voltage at $V_d \to 0$, $V_{\rm ch}$ is the position-dependent channel potential, $N_{\rm ch}$ is the position-dependent carrier density, n is the body factor, V_T is the thermal potential, $a = q/C_{\rm ox}$, q is an electron charge, $C_{\rm ox}$ is the gate oxide capacitance, and $N_0 = N_{\rm inv\_thresh}$ is the value of $N_{\rm inv}$ at $V_g = V_{\rm TH}$ given by [9]

$$N_{\rm inv\_thresh} = \frac{nV_T}{2a} = \frac{nV_TC_{\rm ox}}{2q}. \qquad (2)$$

In the framework of the gradual channel approximation, the drain current can be expressed as

$$I_d(x) = q \cdot W \cdot \mu \cdot N_{\rm ch}(x) \frac{dV_{\rm ch}}{dx} \qquad (3)$$

where W is the channel width and μ is the carrier mobility assumed to be constant. Integrating (3) along the channel, accounting for (1), gives [9]

$$I_d = q\mu \frac{W}{L} \frac{1}{n} \left[nV_T(N_S - N_D) + \frac{a\left(N_S^2 - N_D^2\right)}{2} \right] \qquad (4)$$

where L is the channel length and N_S and N_D are the inversion carrier densities at the source and drain channel edges, respectively. The V_d and V_g dependences are implicitly included in (4) through $N_S(V_g)$ and $N_D(V_g, V_d)$ dependences, which are determined by relation (1) with $V_{\rm ch}$ being equal to $V_s(= 0)$ and V_d, respectively. Note that, in our case of $V_s = 0$, from (1) follows that $N_S(V_g)$ coincides with $N_{\rm inv}(V_g)$ for the uniform carrier distribution along the channel (relation (4) in the companion paper [7]).

A. Impact of Drain Voltage on the Peak Position of d^2I_d/dV_g^2

As follows from (4), the behavior of the drain current derivatives, dI_d/dV_g, d^2I_d/dV_g^2, and d^3I_d/dV_g^3, is governed by the behavior of the derivatives of the carrier densities at the source and drain channel edges, $N_S(V_g)$ and $N_D(V_g, V_d)$. Differentiating (1) with respect to V_g, we obtain

$$\frac{dN_{\rm ch}}{dV_g} = \frac{N_{\rm ch}}{nV_T + aN_{\rm ch}} \qquad (5)$$

$$\frac{d^2N_{\rm ch}}{dV_g^2} = \frac{nV_T \cdot N_{\rm ch}}{(nV_T + aN_{\rm ch})^3}. \qquad (6)$$

From (6) follows that the expressions for d^2N_S/dV_g^2 and d^2N_D/dV_g^2 are identical (which is the consequence of identity of the right-hand sides of (1) for $V_{\rm ch}$ equal to $V_s = 0$ and V_d), and thus, equations emerging from the condition of their maxima by setting their third derivatives to zero are the same. As a result, the values of N_S and N_D corresponding to the maxima of d^2N_S/dV_g^2 and d^2N_D/dV_g^2 are also the same and equal to the threshold carrier density for uniform channel $N_{\rm inv_{thresh}}$ [9]

$$N_S\left(\max N_S''\right) = N_D\left(\max N_D''\right) = N_{\rm inv\_thresh} = \frac{nV_T}{2a}. \quad (7)$$

Combining (5) with (7) yields

$$q\frac{dN_S}{dV_g}\left(\max N_S''\right) = q\frac{dN_D}{dV_g}\left(\max N_D''\right) = \frac{q}{3a} = \frac{C_{\rm ox}}{3}. \quad (8)$$

From (1) follows that $N_{\rm ch}(V_g, V_{\rm ch})$ and $N_D(V_g, V_d)$ dependences are identical to $N_S(V_g) = N_{\rm inv}(V_g)$ but shifted relative to the latter toward higher V_g by $nV_{\rm ch}$ and nV_d, respectively. Thus

$$N_D(V_g, V_d) = N_S(V_g - nV_d). \quad (9)$$

The same is valid for all the derivatives of N_S and N_D in respect to V_g

$$\frac{d^nN_D(V_g, V_d)}{dV_g^n} = \frac{d^nN_S(V_g - nV_d)}{dV_g^n} \quad (10)$$

that is, each derivative of N_D with respect to V_g is completely identical to the corresponding derivative of N_S (or $N_{\rm inv}$) but is shifted along the V_g-axis by nV_d.

Below, we will express the drain current derivatives in terms of the derivatives of N_S and N_D. Differentiating (4) gives

$$\frac{dI_d}{dV_g} = A\left[nV_T\left(\frac{dN_S}{dV_g} - \frac{dN_D}{dV_g}\right) + a\left(N_S\frac{dN_S}{dV_g} - N_D\frac{dN_D}{dV_g}\right)\right]$$
$$= A\left[\frac{dN_S}{dV_g}\left(nV_T + aN_S\right) - \frac{dN_D}{dV_g}\left(nV_T + aN_D\right)\right] \quad (11)$$

with $A = q\mu\cdot(W/L)\cdot(1/n)$. With (5), the relation (11) can be transformed to give

$$\frac{dI_d}{dV_g} \equiv g_m = A(N_S - N_D) = q\frac{W}{L}\mu\cdot n\cdot(N_S - N_D). \quad (12)$$

Differentiating (12) yields

$$\frac{d^2I_d}{dV_g^2} \equiv \frac{dg_m}{dV_g} = A\left[\frac{dN_S}{dV_g} - \frac{dN_D}{dV_g}\right] \quad (13)$$

$$\frac{d^3I_d}{dV_g^3} = A\left[\frac{d^2N_S}{dV_g^2} - \frac{d^2N_D}{dV_g^2}\right]. \quad (14)$$

Now, let us consider in more details the behavior of the drain current derivatives given by (12)–(14), illustrated by Fig. 6(a)–(c), respectively. In Fig. 6, the $N_S(V_g)$ dependence is the inversion carrier density obtained by 1-D classical numerical simulations [11] for a SOI MOS structure with $t_{\rm ox} =$ 1.75 nm, $t_{\rm Si} = 10$ nm, $t_{\rm BOX} = 145$ nm, film doping of $N_A = 10^{15}$ cm^{-3}, and gate work function of 4.7 eV.

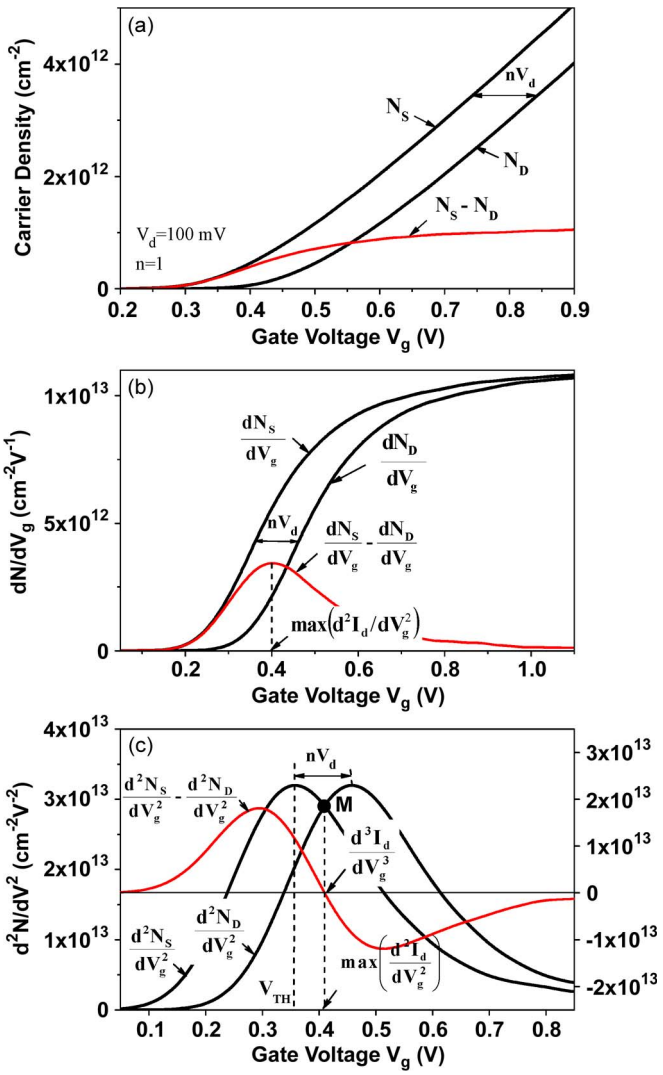

Fig. 6. Illustration of the impact of the drain voltage on the drain current derivatives in terms of the behavior of the carrier densities at the source and drain edges and their derivatives, as described by (12)–(14). (a) $N_S(V_g)$ and $N_D(V_g)$ dependences and their difference which, in accordance with (12), defines the $dI_d/dV_g(V_g, V_d)$ function. (b) dN_S/dV_g and dN_D/dV_g and their difference defining $d^2I_d/dV_g^2(V_g, V_d)$. (c) d^2N_S/dV_g^2 and d^2N_D/dV_g^2 and their difference defining $d^3I_d/dV_g^3(V_g, V_d)$.

According to (12), the $g_m(V_g, V_d) \equiv dI_d/dV_g$ function, which should have an inflection point, is defined by the difference of two identical dependences, $N_S(V_g)$ and $N_D(V_g, V_d)$, shifted along the V_g-axis relative to each other by nV_d [see Fig. 6(a)], each of which steadily grows with monotonically increasing rate, i.e., has no inflection points. Both feature regions of exponential density increase (respectively, below $V_{\rm TH}$ and $V_{\rm TH} + nV_d$) and a linear density increase at higher V_g with the slope $1/a = C_{\rm ox}/q$. The difference $N_S(V_g) - N_D(V_g)$ shows a rise with V_g defined by the growth of $N_S(V_g)$ and a saturation when both $N_S(V_g)$ and $N_D(V_g)$ reach a linear density increase. It is evident that, between growth and saturation regions, there is an inflection point, and an increase of V_d shifts this inflection point to higher V_g. This allows an understanding of the behavior of the experimental $g_m(V_g)$ curves with V_d in Fig. 2.

The behavior of the $dg_m/dV_g\ (V_g, V_d) \equiv d^2I_d/dV_g^2$ dependence with variation of V_d is illustrated in Fig. 6(b). As follows from (13), the d^2I_d/dV_g^2 dependence is formed by the difference of two identical dependences: $dN_S/dV_g(V_g)$ and $dN_D/dV_g(V_g, V_d)$ shifted to higher V_g by nV_d. Note that each alone does not reveal any peak, whereas their difference does: The rise of the $d^2I_d/dV_g^2(V_g, V_d)$ dependence is determined by the increase in dN_S/dV_g, whereas the decay region is determined by the V_d-dependent increase of dN_D/dV_g and saturation of dN_S/dV_g. With an increase of V_d, the rising edge of $d^2I_d/dV_g^2(V_g, V_d)$ will remain unchanged, whereas the falling edge will move to higher V_g. Thus, an increase of V_d naturally shifts the peak position of d^2I_d/dV_g^2 to higher V_g values.

The impact of V_d on the peak position of d^2I_d/dV_g^2 can be better understood by considering the $d^3I_d/dV_g^3(V_g, V_d)$ function illustrated by Fig. 6(c). According to (14), the $d^3I_d/dV_g^3(V_g, V_d)$ dependence is determined by the difference of two bell-shaped dependences, $d^2N_S/dV_g^2(V_g)$ and $d^2N_D/dV_g^2(V_g, V_d)$, having their maxima at the points $V_g = V_{\rm TH}$ and $V_g = V_{\rm TH} + nV_d$, respectively [see Fig. 6(c)]. Thus, the condition of the maximum of d^2I_d/dV_g^2, which is $d^3I_d/dV_g^3 = 0$, may be expressed as

$$\frac{d^2N_S}{dV_g^2}(V_g) = \frac{d^2N_D}{dV_g^2}(V_g, V_d). \tag{15}$$

This means that *the peak position of d^2I_d/dV_g^2 simply corresponds to the intersection point of the $d^2N_S/dV_g^2(V_g)$ and $d^2N_D/dV_g^2(V_g, V_d)$ curves and thus always lies between their maxima, i.e., between $V_{\rm TH}$ and $(V_{\rm TH} + nV_d)$* [see point M in Fig. 6(c)]. Increasing V_d does not change the position of the maximum of $d^2N_S/dV_g^2(V_g)$, which, for $V_s = 0$, lies at $V_g = V_{\rm TH}$, whereas it shifts the maximum of $d^2N_D/dV_g^2(V_g, V_d)$ to higher V_g values by nV_d. Thus, as V_d increases, the deviation of the peak position of d^2I_d/dV_g^2 from $V_{\rm TH}$ increases. The value of this deviation, $\Delta V(\max I_d'') = V_g(\max I_d'') - V_{\rm TH}$, is roughly equal to $nV_d/2$ (more precisely, it slightly exceeds $nV_d/2$ due to some asymmetry of the bell-shaped $d^2N_{\rm inv}/dV_g^2$ curves). It is evident that, when $V_d \to 0$, the peak position of d^2N_D/dV_g^2 approaches to that of d^2N_S/dV_g^2, and thus, the peak position of d^2I_d/dV_g^2 approaches to $V_{\rm TH}$.

The resulting expression for the shift of the peak position of d^2I_d/dV_g^2 relative to $V_{\rm TH}$, $\Delta V_g(\max I_d'') = V_{\rm gm}(V_d) - V_{\rm TH}$, as a function of V_d is

$$\Delta V_g\left(\max I_d''\right) = \frac{4}{9}nV_d - nV_T \ln\left(\frac{1 + e^{\frac{2}{9}\cdot\frac{V_d}{V_T}}}{2}\right) + \frac{nV_T}{2}\left[\frac{2e^{\frac{4}{9}\cdot\frac{V_d}{V_T}}}{1 + e^{\frac{2}{9}\cdot\frac{V_d}{V_T}}} - 1\right]. \tag{16}$$

The detailed derivation of (16) is provided in Appendix A. As follows from (16), the shift of the peak position of d^2I_d/dV_g^2 is determined only by the applied drain voltage V_d and body factor n.

B. Impact of Drain Voltage on the Peak Position of $-d(g_m/I_d)/dV_g$

Using (12) and (4), we can express g_m/I_d as

$$\frac{g_m}{I_d} = \frac{N_S - N_D}{nV_T\left[N_S - N_D + \frac{a\cdot\left(N_S^2 - N_D^2\right)}{2}\right]} \tag{17}$$

which can be rearranged to give

$$\frac{g_m}{I_d}(V_g, V_d) = \frac{1}{nV_T + \frac{a}{2}\left[N_S(V_g) + N_D(V_g, V_d)\right]}. \tag{18}$$

Since both N_S and N_D monotonically increase with V_g, the g_m/I_d function monotonically decreases with V_g, taking its maximum value equal to $1/nV_T$ when N_S and N_D tend to zero. It is readily seen that, at $V_d \to 0$, when $N_D\ (V_g, V_d) \to N_S\ (V_g)$, (18) transforms into

$$\frac{g_m}{I_d}(V_g, V_d \to 0) = \frac{1}{nV_T + aN_S}. \tag{19}$$

Therewith, the derivative of g_m/I_d at $V_d \to 0$ is expressed as

$$\left.\frac{d}{dV_g}\left(\frac{g_m}{I_d}\right)\right|_{V_d \to 0} = -a \cdot \frac{N_S}{(nV_T + aN_S)^3} \tag{20}$$

which, within a factor $(-nV_T/a)$, coincides with $d^2N_S/dV_g^2 = d^2N_{\rm inv}/dV_g^2$ [see (6)]. This means that, at $V_d \to 0$, the position of the maximum of the $[-d(g_m/I_d)/dV_g]$ function coincides with $V_{\rm TH}$. Substituting (7) into (19) gives the value of g_m/I_d at threshold

$$\left.\frac{g_m}{I_d}\right|_{V_d \to 0, V_g = V_{\rm TH}} = \frac{2}{3}\cdot\frac{1}{nV_T} = \frac{2}{3}\left(\frac{g_m}{I_d}\right)_{\max}. \tag{21}$$

Thus, for vanishingly small drain voltages at $V_g = V_{\rm TH}$, g_m/I_d is equal to 2/3 of its maximum value. This finding could be used as an alternative method of the $V_{\rm TH}$ extraction, satisfying the $V_{\rm TH}$ criterion of the maximum of the second derivative of the inversion charge, provided that the transistor is sufficiently free of second-order effects.

Below, we show that, as V_d increases, the gate voltage of the maximum of $-d(g_m/I_d)/dV_g$ tends to a limit. As follows from (1), the $N_D(V_g, V_d)$ dependence can be obtained by the parallel shift of $N_S(V_g)$ by nV_d. Consequently, at sufficiently high V_d, over the whole range of V_g from 0 to $V_g = V_{\rm TH} + nV_d$, the condition $N_D \ll N_S$ will be satisfied. Thus, as V_d increases, the g_m/I_d function described by (18) tends to the limit, which is determined only by the variation of the carrier density at the source edge and is independent of V_d

$$\left[\frac{g_m}{I_d}(V_g)\right]_{\rm lim} = \frac{1}{nV_T + \frac{a}{2}N_S(V_g)}. \tag{22}$$

Equation (22) defines the maximum value of g_m/I_d for each V_g with the increase of V_d from 0 to ∞. Thus, the whole variation of the $g_m/I_d(V_g)$ dependence with V_d lies between the two limiting curves described by (19) and (22), as illustrated by the dashed area in Fig. 7. Since the ratio $N_{\rm Dm}/N_{\rm Sm}$, which governs the transition from (19) to (22),

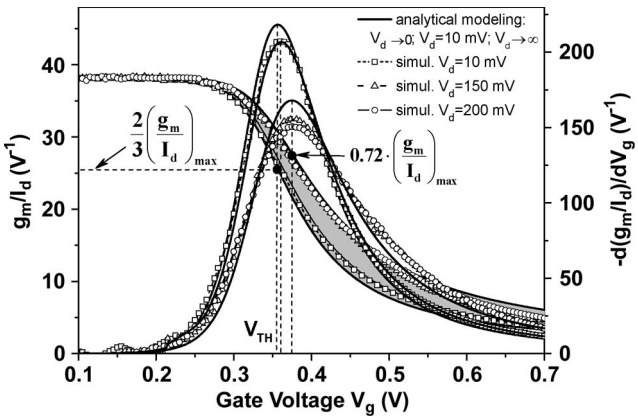

Fig. 7. Comparison of the behavior of the g_m/I_d versus V_g curves and their derivatives at various drain voltages, obtained by Atlas 2-D simulations for UTB SOI MOSFET, featuring $t_{\rm ox} = 1.75$ nm, $t_{\rm Si} = 10$ nm, $t_{\rm BOX} = 145$ nm, and $L = 1$ μm, with the results of modeling for $V_d \to 0$, $V_d = 10$ mV, and $V_d \to\infty$ obtained using (19), (18), and (22), respectively.

is approximately $\sim \exp(-V_d/V_T)$, the position of the maximum of $-d(g_m/I_d)/dV_g$ is expected to be almost saturated at $V_d \geq 3V_T$.

By setting $d^2(g_m/I_d)_{\rm lim}/dV_g^2 = 0$, we get the equation whose solution gives the carrier density at the source edge at the peak position of $-d(g_m/I_d)/dV_g$ in the limiting case, $N_{\rm Sm\_lim}$ (see Appendix B)

$$N_{\rm Sm\_lim} = \frac{nV_T}{a}\left(\frac{\sqrt{17}-1}{4}\right) \tag{23a}$$

or

$$N_{\rm Sm\_lim} = 0.78\cdot\frac{nV_T}{a} \approx \frac{3}{4}\frac{nV_T}{a} = \frac{3}{2}N_{\rm inv\_thresh}. \tag{23b}$$

Substituting (23a) in (1) with $V_{\rm ch} = 0$, we find the limiting value of the V_d-induced shift of the peak position of $[-d(g_m/I_d)/dV_g]$

$$\Delta V_g\left[\max(g_m/I_d)'_{\rm lim}\right] = nV_T\left[\ln\left(\frac{\sqrt{17}-1}{2}\right)+\frac{\sqrt{17}-3}{4}\right] = 0.726\times nV_T. \tag{24}$$

From (24), the maximum V_d-induced shift of the peak position of $d(g_m/I_d)/dV_g$ for an ideal device ($n = 1$) at room temperature is expected to be $\sim$19 mV.

Substituting (23) into (22) yields that, at the limiting position of the maximum of $d(g_m/I_d)/dV_g$, the ratio of g_m/I_d to its maximum value is to be 0.72, which is only slightly higher than that at $V_d \to 0$ when it is $\sim$0.67, as illustrated in Fig. 7.

It is straightforward to show that, in the intermediate range of $V_d (0 < V_d < 3 \div 4\ V_T)$, at the point corresponding to the maximum of $-d(g_m/I_d)/dV_g$, the carrier density at the source edge can be expressed as

$$N_{\rm Sm} = \frac{nV_T}{4a}\left[\sqrt{1+\frac{16}{1+e^{-\frac{3}{2}\frac{V_d}{V_T}}}}-1\right] \tag{25}$$

and finally substituting (25) into (1) with $V_{\rm ch} = 0$, we obtain the expression for the shift of the maximum of $-d(g_m/I_d)/dV_g$ versus V_d

$$\Delta V_g\left[\max\left(-\frac{g_m}{I_d}\right)'\right] = nV_T\left[\ln\left(\frac{\sqrt{1+\frac{16}{1+e^{-\frac{2}{3}\frac{V_d}{V_T}}}}-1}{2}\right)+\frac{\sqrt{1+\frac{16}{1+e^{-\frac{2}{3}\frac{V_d}{V_T}}}}-3}{4}\right]. \tag{26}$$

Note that, at $V_d \to 0$, (26) gives $\Delta V_g[\max(-g_m/I_d)'] = 0$, whereas at $V_d \to \infty$, it results in the limiting shift value given by (24).

It should be noted that, from the point of the mathematical procedure, the $d(g_m/I_d)/dV_g$ method is similar to the second derivative logarithmic (SDL) method, in which $V_{\rm TH}$ is defined as the gate voltage where $d^2(\log I_d)/dV_g^2$ exhibits a minimum [12] since

$$\frac{d}{dV_g}\left(\frac{g_m}{I_d}\right) = \frac{d}{dV_g}\left[\frac{1}{I_d}\left(\frac{dI_d}{dV_g}\right)\right] = \frac{d^2(\ln I_d)}{dV_g^2} = \ln 10\cdot\frac{d^2(\log I_d)}{dV_g^2}.$$

However, physical meanings attributed to both methods are different. For the $d(g_m/I_d)/dV_g$ method, the underlying $V_{\rm TH}$ criterion is shown to be the maximum of $d^2N_{\rm inv}/dV_g^2$, while for the SDL method, it is assumed to be the equality of drift and diffusion currents [12]. As shown in [13], the condition of the equality of drift and diffusion currents corresponds to the point on the $g_m/I_d(V_g)$ curve where g_m/I_d equals 1/2 of its maximum value. However, as shown in this paper, the minimum of $d(g_m/I_d)/dV_g$, and thus the minimum of $d^2(\log I_d)/dV_g^2$), corresponds to the point where the ratio of g_m/I_d to its maximum value is 2/3 at $V_d \to 0$ and increases with V_d to 0.72. This means that, in the general case, in an ideal long-channel MOSFET, *the points, where $d^2(\log I_d)/dV_g^2$ is minimum and where drift and diffusion current components are equal, do not coincide*.

C. Comparison of Modeling Results With Simulation and Experimental Data

In order to verify our modeling derivations, we compare them below with numerical simulations and experimental data.

Atlas 2-D classical simulations have been performed for the n-channel UTB SOI MOSFET with $L = 1$ μm, $t_{\rm ox} = 1.75$ nm, $t_{\rm Si} = 10$ nm, $t_{\rm BOX} = 145$ nm, p-type film and substrate doping of 6.5×10^{14} cm^{-3}, and gate metal work function of 4.7 eV. In simulation, we assumed mobility to be constant and source and substrate to be grounded. The step increment in V_g was 5 mV.

Fig. 7 presents with symbols the g_m/I_d curves and their derivatives obtained by simulations for different V_d's (10, 150, and 200 mV), whereas solid lines represent modeling data for $V_d \to 0$, $V_d = 10$ mV, and $V_d \to\infty$, obtained from (19), (18), and (22), respectively, with $n = 1.02$. The dashed area between the curves for $V_d \to 0$ and $V_d \to\infty$ indicates the whole range of variation of $g_m/I_d(V_g)$ with drain voltage predicted by analytical modeling. One can see a good agreement between modeling

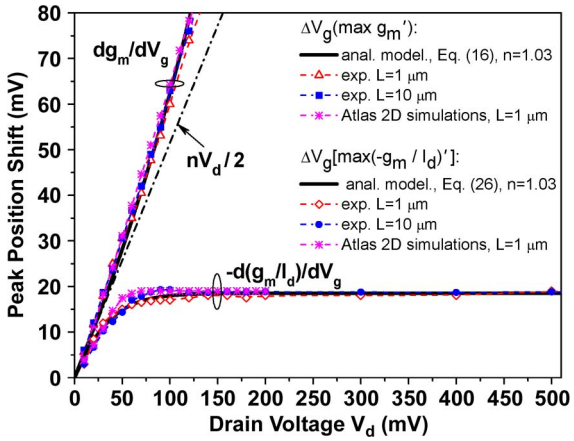

Fig. 8. Comparison of modeling results for the shifts of the peak positions of dg_m/dV_g and $[-d(g_m/I_d)/dV_g]$ versus V_d with experimental and simulation data.

and simulations. The simulated g_m/I_d curve for $V_d = 10$ mV is well reproduced by (18), where the $N_S(V_g)$ and $N_D(V_g)$ dependences were calculated from (1) with $V_{\rm ch} = 0$ and 10 mV, respectively, whereas the curves for $V_d = 150$ and 200 mV around threshold are well fitted by the modeled limiting curve for $V_d \to \infty$ [(22)]. In addition, modeling fits well the peak position shift of the simulated $d(g_m/I_d)/dV_g$ with V_d.

Our model is also in a good agreement with experimental data presented in Section II. It perfectly reproduces all the trends in the behavior of the experimental g_m/I_d curves shown in Fig. 3, namely, the variation around $V_{\rm TH}$ at $V_d < 100$ mV [see Fig. 3(a)] and saturation at higher V_d [see Fig. 3(b)]. The ratio of the experimental g_m/I_d to its maximum value at the peak position of $d(g_m/I_d)/dV_g$ at $V_d = 10$ mV is equal to 0.62. However, taking into account the V_d-induced shift, which, for $V_d = 10$ mV, is expected to be 3.3 mV, we obtain that, at $V_g = V_{\rm TH}$, this ratio is ~0.65, which is in a reasonable agreement with the predicted 2/3. Then, the maximum shift of the peak position of the experimental $-d(g_m/I_d)/dV_g$ with V_d in Fig. 3 is ~20 mV, which corresponds closely to that predicted by (24), i.e., $0.726 \times nV_T \approx 19$ mV (with $n = 1.03$ taken from the measured subthreshold $I_d(V_g)$ characteristics).

It is interesting to note that the saturated peak position of $d(g_m/I_d)/dV_g$ is very close to the saturation threshold voltage $V_{\rm TH\_sat}$ determined by the linear extrapolation of the saturated $\sqrt{I_{d\_\rm sat}(V_g)}$ characteristics. Thus, the $d(g_m/I_d)/dV_g$ method appears to be applicable for the extraction of the saturated threshold voltage $V_{\rm TH\_sat}$.

In Fig. 8, we compare the predictions of analytical modeling for the shifts of the peak positions of $-d(g_m/I_d)/dV_g$ and dg_m/dV_g versus V_d ((26) and (16), respectively) with experimental and simulation data. For ease of comparison, experimental and simulation data in Fig. 8 are matched with modeled results at $V_d = 10$ mV.

It should be noted that simulated and experimental devices have different structural parameters but both feature near-ideal subthreshold factor n, being 1.02 and 1.03, respectively. Thus, from our model, it is expected that the peak position shifts of $-d(g_m/I_d)/dV_g$ and dg_m/dV_g, depending only on the factor n, for the simulated and experimental devices should be approximately the same, which is what we see in Fig. 8. This provides additional evidence in favor of our model.

As is seen from Fig. 8, (16) nicely fits the experimental and simulated V_d dependence of the peak position shift of dg_m/dV_g, at least for $V_d \le 100$ mV (that is, in the usable range of the transconductance change method), whereas (26) reproduces well the behavior of the peak position shift of the experimental and simulated $d(g_m/I_d)/dV_g$ in the whole range of V_d. One can see that the shift of the peak position with V_d for dg_m/dV_g exceeds $nV_d/2$, whereas for $d(g_m/I_d)/dV_g$, it is smaller and rapidly saturates at a level of ~19 mV, i.e., 0.73 V_T, being in excellent agreement with (24). We emphasize that the aforementioned good agreement of analytical modeling with simulation and experimental results is obtained without introducing any fitting parameter.

IV. Conclusion

The effect of the drain voltage on $V_{\rm TH}$ extraction in a long-channel MOSFET from the peak positions of $-d(g_m/I_d)/dV_g$ and dg_m/dV_g has been thoroughly studied, using experimental data, 2-D numerical simulations, and analytical modeling based on the UCCM. It was shown that, although both methods rely on the same $V_{\rm TH}$ criterion (of the maximum of the second derivative of the inversion charge), they feature radically different behaviors in respect of the drain voltage. The dg_m/dV_g method yields a $V_{\rm TH}$ value which monotonically increases with drain voltage. In contrast, for the $d(g_m/I_d)/dV_g$ method, this increase is smaller and rapidly saturates with drain voltage (when V_d exceeds $3 \div 4$ V_T), being in the limit $0.726 \times nV_T$. Analytical expressions for the aforementioned V_d dependences for both methods have been derived. Modeling results revealed a very good agreement with numerical simulation and experimental data, without any fitting parameters. Thus, the obtained expressions can be used for the correction of the $V_{\rm TH}$ values in the long-channel devices extracted by dg_m/dV_g and $d(g_m/I_d)/dV_g$ methods.

It was also shown that, at the position of the extremum of $d(g_m/I_d)/dV_g$ at vanishingly small drain voltage and ideal MOSFET operation, the value of g_m/I_d is equal to 2/3 of its maximum value. This finding can be used as an alternative quick method for the $V_{\rm TH}$ extraction. However, such $V_{\rm TH}$ extraction is possible only when the $g_m/I_d(V_g)$ curve has a clearly defined plateau in the range of the maximum, whereas it is frequently distorted, for example, due to GIDL, short-channel effects, or gate-voltage-dependent mobility. Thus, the $d(g_m/I_d)/dV_g$ method seems to be more preferable since it only uses the data measured around threshold and hence minimizes assumptions of ideal behaviors in weak or strong inversion.

Appendix A
Derivation of (16)

Analytical expressions for the gate voltage of the maximum of d^2I_d/dV_g^2 and its shift versus V_d are obtained by solving a system of two equations. The first is obtained by setting in (14) $d^3I_d/dV_g^3 = 0$, which, taking into account (6), gives

$$N_{\rm Sm}(nV_T + aN_{\rm Dm})^3 = N_{\rm Dm}(nV_T + aN_{\rm Sm})^3 \qquad \text{(A1)}$$

where $N_{\rm Sm}$ and $N_{\rm Dm}$ are the carrier densities at the source and drain edges at the gate voltage $V_{\rm gm}$ corresponding to the maximum of d^2I_d/dV_g^2 [point M in Fig. 6(c)], which are determined from (1) with $V_{\rm ch}$ equal to $V_S = 0$ and V_d, respectively, and $V_g = V_{\rm gm}$

$$V_{\rm gm} - V_{\rm TH} = nV_T \ln\left(\frac{N_{\rm Sm}}{N_0}\right) + a(N_{\rm Sm} - N_0) \quad \text{(A2)}$$

$$V_{\rm gm} - V_{\rm TH} - nV_d = nV_T \ln\left(\frac{N_{\rm Dm}}{N_0}\right) + a(N_{\rm Dm} - N_0). \quad \text{(A3)}$$

The second expression containing the V_d dependence is obtained by subtracting (A3) from (A2)

$$nV_d = nV_T \ln\left(\frac{N_{\rm Sm}}{N_{\rm Dm}}\right) + a(N_{\rm Sm} - N_{\rm Dm}). \quad \text{(A4)}$$

The exponentiation of (A4) yields

$$\frac{N_{\rm Sm}}{N_{\rm Dm}} = e^{\frac{nV_d - a(N_{\rm Sm} - N_{\rm Dm})}{nV_T}}. \quad \text{(A5)}$$

By substituting (A5) into (A1), we get the equation whose solution gives

$$N_{\rm Sm} = \frac{nV_T}{a} \cdot \frac{e^{\frac{2}{3}\cdot\frac{nV_d - a(N_{\rm Sm} - N_{\rm Dm})}{nV_T}}}{e^{\frac{1}{3}\cdot\frac{nV_d - a(N_{\rm Sm} - N_{\rm Dm})}{nV_T}} + 1}. \quad \text{(A6)}$$

Equation (A6) can be simplified taking into account the following. From the comparison of (A2) and (A3) follows that nV_d corresponds to the total V_g increase which causes the variation of N_S from $N_S = N_{\rm Dm}$ to $N_S = N_{\rm Sm}$, whereas $a(N_{\rm Sm} - N_{\rm Dm})$ in (A6) represents the part of the V_g increase related to the voltage drop on the gate dielectric, which, at the points of the maxima of d^2N_S/dV_g^2 and d^2N_D/dV_g^2 in accordance with (8), is 1/3 from the total gate voltage increase. Thus, we can write

$$a(N_{\rm Sm} - N_{\rm Dm}) = \frac{1}{3}nV_d. \quad \text{(A7)}$$

Substituting (A7) into (A6) yields

$$N_{\rm Sm}(V_d) = \frac{nV_T}{a} \cdot \frac{e^{\frac{4}{9}\cdot\frac{V_d}{V_T}}}{1 + e^{\frac{2}{9}\cdot\frac{V_d}{V_T}}}. \quad \text{(A8)}$$

Note that, when $V_d \to 0$, (A8) gives $N_{\rm Sm} = nV_T/(2a) = N_{\rm inv\_thresh}$ Substituting (A8) into (A2), we get

$$\Delta V_g\,(\max I_d'') = \frac{4}{9}nV_d - nV_T \ln\left(\frac{1 + e^{\frac{2}{9}\cdot\frac{V_d}{V_T}}}{2}\right) + \frac{nV_T}{2}\left[\frac{2e^{\frac{4}{9}\cdot\frac{V_d}{V_T}}}{1 + e^{\frac{2}{9}\cdot\frac{V_d}{V_T}}} - 1\right]. \quad \text{(A9)}$$

APPENDIX B
DERIVATION OF (23)

From (22), the derivative of the limiting g_m/I_d function corresponding to $V_d \to \infty$ is expressed as

$$\frac{d}{dV_g}\left[\frac{g_m}{I_d}\right]_{\rm lim} = \frac{-\frac{a}{2}}{\left(nV_T + \frac{a}{2}N_S\right)^2} \cdot \frac{dN_S}{dV_g} \quad \text{(B1)}$$

which, taking into account (5), gives

$$\frac{d}{dV_g}\left[\frac{g_m}{I_d}\right]_{\rm lim} = -\frac{a}{2} \cdot \frac{N_S}{\left(nV_T + \frac{a}{2}N_S\right)^2 (nV_T + aN_S)}. \quad \text{(B2)}$$

Let us denote the denominator in (B2) as D

$$D = \left(nV_T + \frac{a}{2}N_S\right)^2 (nV_T + aN_S) = (nV_T)^3 + 2(nV_T)^2 aN_S + \frac{5}{4}(nV_T) \cdot a^2N_S^2 + \frac{a^3N_S^3}{4}. \quad \text{(B3)}$$

Then, the derivative of (B2) can be written as

$$\frac{d^2}{dV_g^2}\left[\frac{g_m}{I_d}\right]_{\rm lim} = -\frac{a}{2}\frac{D - N_S \cdot \frac{dD}{dN_S}}{D^2} \cdot \frac{dN_S}{dV_g}. \quad \text{(B4)}$$

With (5) and (B3), (B4) becomes

$$\frac{d^2}{dV_g^2}\left[\frac{g_m}{I_d}\right]_{\rm lim} = -\frac{a}{2} \cdot \frac{(nV_T)^3 - \frac{5}{4}(nV_T) \cdot a^2N_S^2 - \frac{1}{2}a^3N_S^3}{\left(nV_T + \frac{a}{2}N_S\right)^4 (nV_T + aN_S)^3}. \quad \text{(B5)}$$

By equating (B5) to 0 and denoting the carrier density at the source edge at the point of the maximum of $[-d(g_m/I_d)/dV_g]_{\rm lim}$ as $N_{\rm Sm\_lim}$, we obtain the following equation of the third degree for $N_{\rm Sm\_lim}$:

$$(nV_T)^3 - \frac{5}{4}(nV_T) \cdot a^2N_{\rm Sm\_lim}^2 - \frac{1}{2}a^3N_{\rm Sm\_lim}^3 = 0 \quad \text{(B6)}$$

which can be easily transformed into a quadratic equation. The rearrangement of the terms in (B6) yields

$$(nV_T)\left[(nV_T)^2 - \frac{1}{4}a^2N_{\rm Sm\_lim}^2\right] - a^2N_{\rm Sm\_lim}^2\left[nV_T + \frac{1}{2}aN_{\rm Sm\_lim}\right] = 0$$

which can be transformed to give

$$\left(nV_T + \frac{1}{2}aN_{\rm Sm\_lim}\right) \times \left[nV_T\left(nV_T - \frac{1}{2}aN_{\rm Sm\_lim}\right) - a^2N_{\rm Sm\_lim}^2\right] = 0. \quad \text{(B7)}$$

Since the expression in the first bracket cannot be equal zero at no conditions, from (B7), we get

$$a^2N_{\rm Sm\_lim}^2 + \frac{1}{2}(nV_T) \cdot aN_{\rm Sm\_lim} - \left(\frac{nV_T}{a}\right)^2 = 0. \quad \text{(B8)}$$

Finally, dividing (B8) by a^2 gives

$$N_{\rm Sm\_lim}^2 + \frac{nV_T}{2a} \cdot N_{\rm Sm\_lim} - \left(\frac{nV_T}{a}\right)^2 = 0 \quad \text{(B9)}$$

which yields

$$N_{\rm Sm\_lim} = \frac{nV_T}{a}\left(\frac{\sqrt{17} - 1}{4}\right). \quad \text{(B10)}$$

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REFERENCES

[1] A. B. Fowler and A. M. Hartstein, "Techniques for determining threshold," *Surface Sci.*, vol. 98, no. 1–3, pp. 169–172, Aug. 1980.
[2] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electron. Lett.*, vol. 24, no. 9, pp. 543–545, Apr. 1988.
[3] H. S. Wong, M. H. White, T. J. Krutsick, and R. V. Booth, "Modeling of transconductance degradation and extraction of threshold voltage in thin oxide MOSFET," *Solid State Electron.*, vol. 30, no. 9, pp. 953–968, Sep. 1987.
[4] A. Ortiz-Conde, F. J. García Sánchez, J. J. Liou, A. Cerdeira, M. Estrada, and Y. Yue, "A review of recent MOSFET threshold voltage extraction methods," *Microelectron. Reliab.*, vol. 42, no. 4/5, pp. 583–596, May 2002.
[5] F. J. García Sánchez, A. Ortiz-Conde, and J. Muci, "Understanding threshold voltage in undoped-body MOSFETs: An appraisal of various criteria," *Microelectron. Reliab.*, vol. 46, no. 5/6, pp. 731–742, May/Jun. 2006.
[6] D. Flandre, V. Kilchytska, and T. Rudenko, " g_m/I_d method for threshold voltage extraction applicable in advanced MOSFETs with non-linear behavior above threshold," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 930–932, Sep. 2010.
[7] T. Rudenko, V. Kilchytska, M. K. Md Arshad, J.-P. Raskin, A. Nazarov, and D. Flandre, "On the MOSFET threshold voltage extraction by transconductance change and transconductance-to-current ratio change methods: Part I—Effect of gate-voltage-dependent mobility," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4172–4179, Dec. 2011.
[8] T. Rudenko, V. Kilchytska, M. K. Md Arshad, J.-P. Raskin, A. Nazarov, and D. Flandre, "Influence of drain voltage on MOSFET threshold voltage determination by transconductance change and g_m/I_d methods," in *Proc. ULIS*, 2011, pp. 150–153.
[9] C.-K. Park, C.-Y. Lee, K. Lee, B. Y. Moon, Y. H. Byun, and M. Shur, "A unified current-voltage model for long-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 38, no. 2, pp. 399–406, Feb. 1991.
[10] F. Andrieu, O. Faynot, X. Garros, C. Lafond, C. Buj-Dufournet, L. Tosti, S. Minoret, V. Vidal, J. C. Barbe, F. Allain, E. Rouchouze, L. Vandroux, V. Cosnier, M. Casse, V. Delaye, C. Carabasse, M. Burdin, G. Rolland, B. Guillaumot, J. P. Colonna, P. Besson, L. Brevard, D. Mariolle, P. Holliger, A. Vandooren, C. Fenouillet-Beranger, F. Martin, and S. Deleonibus, "Comparative scalability of PVD and CVD TiN on HfO_2 as a metal gate stack for FDSOI cMOSFETs down to 25nm gate length and width," in *IEDM Tech. Dig.*, 2006, pp. 641–644.
[11] Schred Simulation Tool. [Online]. Available: http://nanohub.org
[12] K. Aoyama, "A method for extracting the threshold voltage of MOSFETs based on current components," in *Simulation of Semiconductor Devices and Processes*, H. Ryssel and P. Pichler, Eds. Vienna, Austria: Springer-Verlag, Sep. 1995, pp. 118–121.
[13] A. A. Cunha, M. A. Pavanello, R. D. Trevisoli, C. Galup-Montoro, and M. C. Schneider, "Direct determination of threshold voltage condition in DG-MOSFETs from the g_m/I_D curve," *Solid State Electron.*, vol. 56, no. 1, pp. 89–94, Feb. 2011.

Tamara Rudenko, photograph and biography not available at the time of publication.

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